DECLARATION

I, the undersigned, of 17-15 Shinmachi, Kaizuka-shi, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **2003-404895**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

Y. Kitamura

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Dated: November 19, 2008

[Name of the Document] Claims

[Claim 1]

A transistor comprising:

a source electrode and a drain electrode arranged in mutually opposing relation;

a semiconductor film comprising at least one layer disposed between the source electrode and the drain electrode;

a gate electrode disposed in adjacent relation to the semiconductor film; and

a gate insulating film disposed between the gate electrode and each of the source electrode, the drain electrode, and the semiconductor film, wherein

a concentration of fluorine contained in the gate insulating film is 1×10^{20} atoms/cm^3 or less.

[Claim 2]

The transistor of claim 1, wherein the concentration of the contained fluorine is 1×10^{19} atoms/cm^3 or less.

[Claim 3]

The transistor of claim 1, which is of a field-effect type.

[Claim 4]

The transistor of claim 1, wherein the gate insulating film is an amorphous silicon nitride film.

[Claim 5]

The transistor of claim 1, wherein the gate insulating film is deposited by a CVD method.

[Claim 6]

A CVD apparatus used to deposit the gate insulating film in the transistor of any one of claims 1, 2, 3, 4 and 5, the CVD apparatus comprising:

an electrode having a plurality of gas supply holes and disposed in a reaction chamber, wherein

a surface of the electrode is composed of a non-porous layer.

[Claim 7]

A transistor comprising the gate insulating film deposited by using the CVD apparatus of claim 6.

[Claim 8]

A liquid crystal display device comprising the transistor of claim 7 as a switching element for a pixel electrode portion.

[Name of the Document] Specification

[Title of the Invention] TRANSISTOR AND CVD APPARATUS USED TO DEPOSIT GATE INSLATING FILM THEREOF

[Technical Field]

[0001]

The present invention relates to an improvement in a gate insulating film of a transistor and, more particularly, to a method for reducing a concentration of fluorine contained in a gate insulating film deposited by using a plasma CVD apparatus.

[Background Art]

[0002]

Among field-effect transistors each of which typically comprises at least a gate electrode, a gate insulating film, a semiconductor film, a source electrode and a drain electrode, a field-effect thin-film transistor comprising an amorphous silicon nitride film deposited by a CVD method as the gate insulating film has excellent ON/OFF-state current characteristics so that, in recent years, it has been used also as a switching element for a liquid crystal display device or the like.

[0003]

When the amorphous silicon nitride film is deposited, for example, by using a plasma CVD apparatus, cleaning of the inside of a reaction chamber of the CVD apparatus is performed by using a gas such as NF_3, CF_4, or SF_6 in each given deposition cycle to improve the maintenance property of the CVD apparatus and thereby improve the operability thereof. At this time, if fluorine as one component of the cleaning gas remains in the reaction chamber and is caught in the film being deposited, it causes the problem of significantly degrading the transistor characteristics.

[0004]

As a method for solving this problem, Patent Gazette 1 discloses use of a method other than the CVD method for the reduction of the concentration of fluorine contained in an insulating substrate protecting film in contact with the semiconductor film. As conventional means for reducing the concentration of fluorine contained in the gate insulating film formed by a plasma CVD method, Patent Gazette 2 discloses the removal of residual fluorine by generating a hydrogen plasma after the cleaning of the reaction chamber. It is reported that, by reducing the concentration of the contained fluorine to 1.0×10^{19} atoms/cm^3 or less, an increase in the amount of shift in threshold voltage when the transistor is operated for 10 minutes can be reduced and the reliability of the transistor can be thereby improved.

[Patent Gazette 1] Japanese Laid-Open Patent Publication No. 2002-329869 (page 2, FIG. 1)

[Patent Gazette 2] Japanese Laid-Open Patent Publication No. 2003-124469 (page 2, FIG. 1)

[Disclosure of the Invention]

[Problem to be solved by the Invention]

[0005]

In the method disclosed in Patent Gazette 2, however, evaluation is performed during short-period driving that continues for only 10 minutes. Therefore, it is unknown whether or not the transistor can provide excellent reliability even when it is continuously driven for a long period of time, like a transistor as a switching element for a pixel electrode in a liquid crystal display device.

[0006]

In the method which reduces the residual fluorine in the reaction chamber therefrom by the hydrogen plasma process, a sufficient effect may not be obtained

occasionally depending on the process conditions. Accordingly, it is difficult to stably maintain the excellent characteristics in the reaction chamber.

[0007]

The present invention has been achieved in view of the foregoing circumstances. When a transistor whose gate electrode is deposited by using a CVD apparatus is used as a switching element for a pixel electrode in a liquid crystal display device, a primary object of the invention is to optimize an upper limit value of the fluorine concentration in the gate electrode and achieve the reduction of the fluorine concentration with ease.

[Means of Solving the Problem]

[0008]

To attain the object, the present invention focuses attention on the reduction of the concentration of fluorine contained in the gate insulating film of the transistor to 1×10^{20} atoms/cm^3 or less, preferably to 1×10^{19} atoms/cm^3 or less.

[0009]

As specific means for implementing the reduction in the concentration of the contained fluorine, the surface of an electrode is composed of a non-porous layer in the reaction chamber of the CVD apparatus.

[0010]

As a result, carriers trapped by fluorine at the interface of the gate insulating film in contact with the semiconductor film are reduced so that the ON-state current characteristic of the transistor is improved. At the same time, fluorine ions in the gate insulating film are reduced so that the threshold characteristic of the transistor is improved.

[0011]

In addition, the root cause of the remaining of fluorine in the porous layer, e.g., formed on the surface of the electrode in the reaction chamber by an anodic oxidation

process for forming a protective film can be removed. Compared with the case where the process of removing residual fluorine by using a hydrogen plasma is performed, the production of a faulty transistor resulting from insufficient removal of fluorine due to variations in process conditions and the resultant reduction in yield can be suppressed.

[Effect of the Invention]

[0012]

By adjusting the concentration of fluorine contained in the gate insulating film to 1×10^{20} atoms/cm^3 or less, preferably to 1×10^{19} atoms/cm^3 or less, the present invention not only allows excellent initial characteristics to be obtained but also allows an improvement in reliability even when a transistor is continuously driven for a long period of time at a relative high temperature, as in the case where it is used in a liquid crystal display device. Further, when the gate insulating film is deposited by using a CVD apparatus, the surface of an electrode is composed of a non-porous layer in the reaction chamber. As a result, fluorine in the cleaning gas is less likely to remain in the reaction chamber. Therefore, the production of a faulty transistor resulting from insufficient removal of fluorine and the resultant reduction in yield can be suppressed.

[Best Mode for Carrying Out the Invention]

[0013]

Referring to the drawings, the embodiment of the present invention will be described herein below. It is to be noted that the present invention is not limited to the following embodiment.

[0014]

FIG. **1** schematically shows a cross section of a field-effect thin-film transistor according to the present embodiment. The transistor is used as, e.g., a switching element for a pixel electrode portion in a liquid crystal display device.

[0015]

The foregoing transistor comprises an insulating substrate (**1**) made of, e.g., glass or the like. A gate electrode (**2**) made of Ta, Al, Mo, or the like is formed on the substrate (**1**). A gate insulating film (**3**) composed of, e.g., an amorphous silicon nitride film with a thickness of, e.g., 4000 Å is formed on the gate electrode (**2**) to cover substantially the entire surface of the substrate (**1**). An amorphous silicon semiconductor film (**4**) as a semiconductor film with a thickness of, e.g., 2000 Å is formed on the gate insulating film (**3**) with the portion thereof corresponding to the gate electrode (**2**) being disposed at the center. A pair of n^+ amorphous silicon semiconductor films (**5**) each having a thickness of, e.g., 500 Å and doped with phosphorus are formed on the two regions of the amorphous silicon semiconductor film (**4**) with the gate electrode (**2**) interposed therebetween to serve as semiconductor films other than the amorphous silicon semiconductor film (**4**). A source electrode (**6**) and a drain electrode (**7**) each made of Ti, Mo, Al, or the like are formed over the individual n^+ amorphous silicon semiconductor films (**5**) and the respective portions of the gate insulating film (**3**) continued thereto.

[0016]

A description will be given next to the process steps of fabricating the transistor thus constituted. First, the gate electrode (**2**) is formed on the substrate (**1**) through deposition and patterning. Then, a diode parallel-plate plasma-enhanced CVD apparatus is used and, after the cleaning of the reaction chamber thereof using NF_3 gas, the gate insulating film (**3**) is deposited. Thereafter, a first semiconductor film for obtaining the amorphous silicon semiconductor film (**4**) and a second semiconductor film for obtaining the n^+ amorphous silicon semiconductor films (**5**) are deposited individually. Then, the first and second semiconductor films are patterned into an island configuration to form the amorphous silicon semiconductor film (**4**) first.

[0017]

Further, the source electrode (**6**) and the drain electrode (**7**) are formed through deposition and patterning. Then, by using the pattern of the source electrode (**6**) and the drain electrode (**7**), etching for dividing the second semiconductor film is performed with respect thereto to form the n^+ amorphous silicon semiconductor films (**5**). By the process described above, the field-effect thin-film transistor is completed.

[0018]

A description will be given herein below to the reaction chamber of the plasma CVD apparatus mentioned above with reference to FIG. **2**. In the reaction chamber (**50**), an anode (**52**) made of aluminum and having a large number of gas supply holes (**51**) is disposed. Unlike in the conventional case, an anodic oxidation process for forming a protective film has not been performed with respect to the surface of the anode (**52**). Accordingly, as schematically shown in enlarged relation in FIG. **3**, the surface of the anode (**52**) is composed of an aluminum layer (**70**) as a non-porous film which is exposed in an unprocessed state.

[0019]

Specifically, in the conventional case, an anodic oxidation protective film (**61**) made of alumite is formed on the surface of the aluminum layer (**70**) by the anodic oxidation process for forming the protective film, as schematically shown in FIG. **4**. Because the anodic oxidation protective film (**61**) is porous, fluorine is likely to be trapped by the insides of fine holes therein, which causes a large amount of fluorine to remain in the reaction chamber (**51**) after cleaning. By contrast, the present embodiment has eliminated the root cause described above by forming the aluminum layer (**70**) as the surface of the anode (**52**), i.e., by not forming the anodic oxidation protective film (**61**) as formed conventionally on the surface of the aluminum layer (**70**).

[0020]

For comparison, by using a conventional CVD apparatus in which the surface of the anode (**52**) is composed of the anodic oxidation protective film (**61**), cleaning of the inside of the reaction chamber (**50**) was performed and then a hydrogen plasma process was performed continuously for 60 seconds under conditions such that the output of a radio-frequency power source was 1000 W and the flow rate of gas was 3L/min. As a result, the concentration of fluorine contained in the gate insulating film (**3**) was 3×10^{20} atoms/cm^3. By contrast, in the present embodiment, values of 7×10^{18} to 1×10^{19} atoms/cm^3 were steadily obtained under the same conditions.

[0021]

- Experimental Examples –

A description will be given herein below to an experiment performed to examine the concentration [Unit: atoms/cm^3] of fluorine contained in the gate insulating film of a transistor and the respective initial characteristics of the threshold (Vth [Unit: V]) and ON-state current (Ion [Unit: nA]) thereof. As for the concentration of the contained fluorine, it was determined by depositing an amorphous silicon nitride film under the same conditions as for a gate insulating film on a silicon wafer and measuring the concentration of fluorine contained in the amorphous silicon nitride film by secondary ion mass spectrometry (SIMS). As the transistor, a transistor in which the ratio between the channel width W and the channel length L was W/L = 4 was used.

[0022]

The characteristic view of FIG. **5** shows the initial characteristic between the concentration of fluorine contained in the gate insulating film and the threshold voltage of the transistor. The characteristic view of FIG. **6** shows the initial characteristic between the concentration of fluorine contained in the gate insulating film and the ON-state current

characteristic of the transistor.

[0023]

From the drawings, it will be understood that the initial transistor characteristics are excellent provided that the concentration of the contained fluorine is 1×10^{20} atoms/cm^3 or less, preferably 1×10^{19} atoms/cm^3 or less.

[0024]

A description will be given next to an experiment performed to examine the relationship between the concentration of fluorine contained in the gate insulating film and the reliability of the transistor during the long-period driving thereof at a high temperature.

[0025]

In the conventional case (see Patent Gazette 2), the reliability was evaluated under conditions such that each of the source and drain was grounded, the gate DC voltage was 30 V, and the drive time was 10 minutes in an environment where the temperature was 25.0 ± 3.0 °C. However, when a field-effect thin-film transistor is applied to, e.g., a liquid crystal display device, the guarantee of the operation at a higher temperature for a longer period of time is requested so that the evaluation of the reliability was performed herein under conditions such that each of the source/drain electrodes was grounded, the gate DC voltage was 15 V, and the drive time was 500 hours in an environment where the temperature was 80.0 ± 3.0 °C.

[0026]

As an index for judging the reliability, an amount of shift ΔVth [Unit: V] as a value obtained by subtracting the threshold voltage after a reliability evaluation test from the initial threshold voltage of the transistor was evaluated. As a result, in the transistor in which the concentration of the contained fluorine was 2.7×10^{20} atoms/cm^3, the amount of shift was ΔVth = 5.0 V, while ΔVth = 3.0 V was measured in the transistor in which the

concentration of the contained fluorine was 1.0×10^{20} atoms/cm^3. This proved that the reliability under high-temperature and long-period conditions improved more greatly as the concentration of fluorine contained in the gate insulating film was lower.

[Brief Description of the Drawings]

[0027]

[FIG. 1]

FIG. **1** is a cross-sectional view schematically showing an overall structure of a field-effect thin-film transistor according to an embodiment of the present invention.

[FIG. 2]

FIG. **2** is a schematic view showing an overall structure of a CVD apparatus used to deposit a gate insulating film.

[FIG. 3]

FIG. **3** is a cross-sectional view schematically showing a structure of a surface of an anode in the reaction chamber of the CVD apparatus.

[FIG. 4]

FIG. **4** is a view schematically showing a structure of a surface of an anode in the reaction chamber of a conventional CVD apparatus, which corresponds to FIG. **3**.

[FIG. 5]

FIG. **5** is a characteristic view showing the relationship between the concentration of fluorine contained in a gate insulating film and the threshold voltage of a transistor.

[FIG. 6]

FIG. **6** is a characteristic view showing the relationship between the concentration of fluorine contained in the gate insulating film and the ON-state current characteristic of the transistor.

[Description of Numerals]

[0028]

(2) Gate Electrode

(3) Gate Insulating Film

(4) Amorphous Silicon Semiconductor Film (Semiconductor Film)

(5) n^+ Amorphous Silicon Semiconductor Film (Semiconductor Film)

(6) Source Electrode

(7) Drain Electrode

(50) Reaction Chamber

(51) Gas Supply Hole

(52) Anode (Electrode)

(70) Aluminum Layer (Non-Porous Layer)

[Name of the Document] Abstract

[Summary]

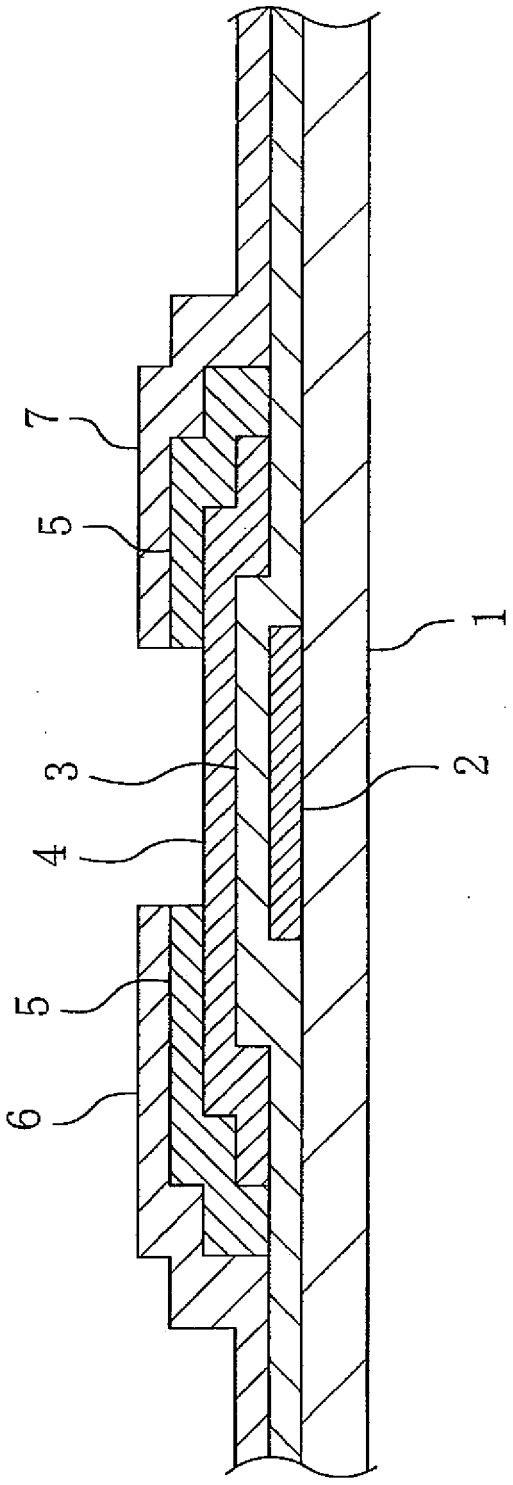
[Purpose] When a transistor whose gate electrode is deposited by using a CVD apparatus is used as a switching element for a pixel electrode in a liquid crystal display device, the present invention allows optimizing an upper limit value of the concentration of fluorine contained in a gate insulating film (**3**) derived from fluorine in a cleaning gas in a reaction chamber and achieving the reduction of the fluorine concentration with ease.

[Solution] The surface of an electrode in a reaction chamber of the CVD apparatus is composed of a non-porous layer so that fluorine in the cleaning gas is less likely to remain in the reaction chamber. The concentration of fluorine contained in the gate insulating film (**3**) is reduced to 1.0×10^{20} atoms/cm^3 or less, preferably to 1×10^{19} atoms/cm^3 or less.

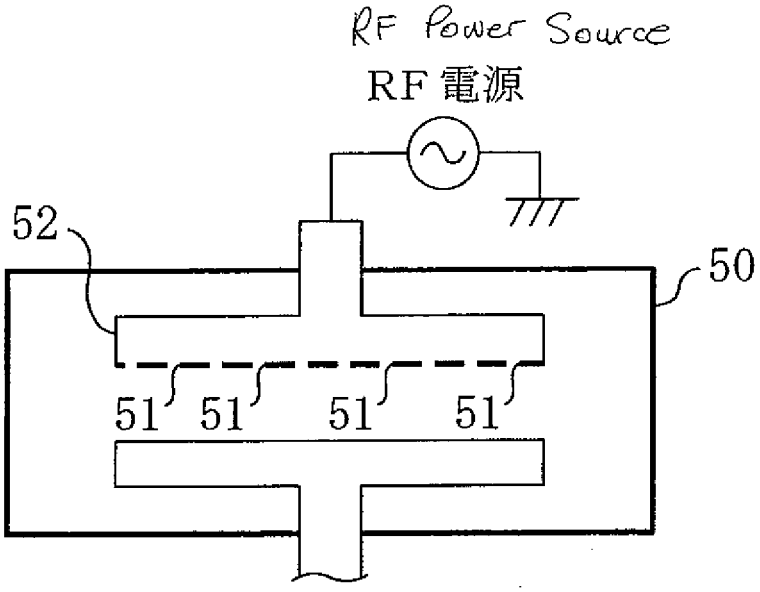
[Selected Figure] FIG. **1**

【書類名】図面 [Name of the Document] Drawing

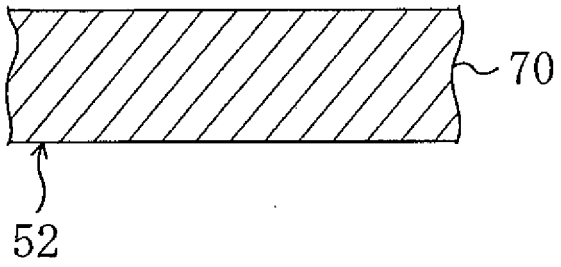
【図1】[FIG. 1]



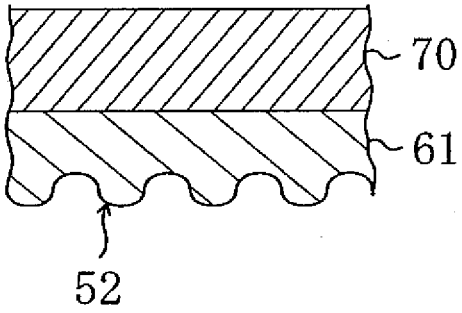
【図２】[FIG. 2]



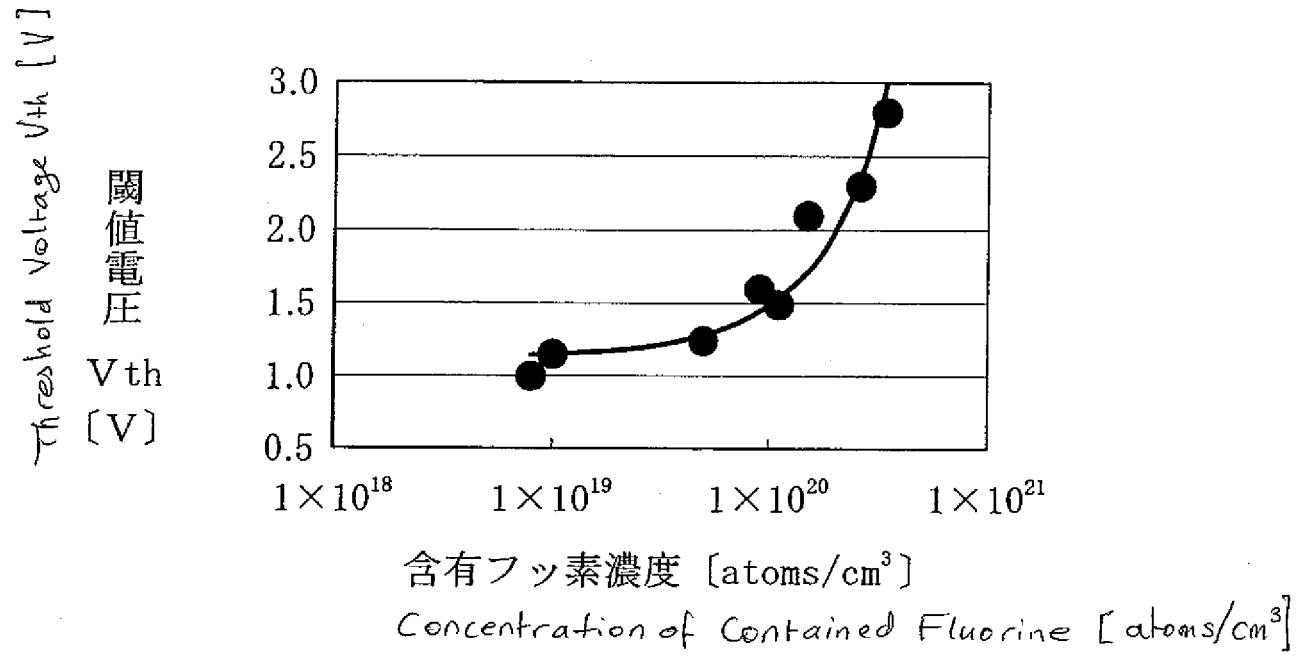
【図３】 [FIG. 3]



【図４】 [FIG. 4]



【図5】[FIG. 5]



【図6】[FIG. 6]